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OPRA Decode at 400Gbps

OVERVIEW

The OPRA (Options Price Reporting Authority) market data feed is a vital source of information for options traders looking to monitor real-time market activity and make timely trade decisions. The performance and speed of this feed is crucial to clients looking for trading success. As the volume of option trading increases, infrastructure providers must ensure quality standards are maintained, and as such are being pushed towards higher bandwidth networking, with 100GbE and 400GbE under consideration.

THE CHALLENGES OF HANDLING 400G

At 400GbE, data widths increase and clock periods decrease, meaning more data can be delivered faster. An average sized OPRA packet, Eth/VLAN/IP/UDP/OPRA with 10 short equity and index quote messages, is approximately 378-bytes. Compared to 10GbE, which provides a 32-bit bus on a 312.5MHz clock, or 100GbE which provides 512-bits at 322.2MHz, 400GbE delivers 1024-bits at over 400MHz. The increased bus size enables an entire 378-byte frame to be received and processed in just 3 clock cycles, compared to 95 clock cycles required for the same frame at 10GbE.

	10G	25G	100G	400G
Standard	IEEE 802.3ae (2002)	IEEE 802.3by (2016)	IEEE 802.3ba (2010)	IEEE 802.3bs (2017)
Bus Width (bits)	32	64	512	1024
Clock Speed (MHz)	312.5	390.625	322.266	415.039
Clock Period (ns)	3.2	2.56	3.10	2.409
Time to Process 378-byte Frame (ns)	304	122.88	18.6	7.23

Additionally, 400GbE uses a segmented interface. There are 16 offsets (or segments) within the interface, meaning a packet can start at any available offset. This capability allows a system to receive more than one packet in a single clock cycle. Based upon the packet size of 378-bytes, in 1ms 10GbE can deliver 3289 packets. However, at 400G an average of 138,346 OPRA packets are received. Software solutions simply cannot cope with this 'firehose' of data. Therefore, bespoke FPGA implementations are essential to handle the sheer volume of data processing required on every clock cycle.

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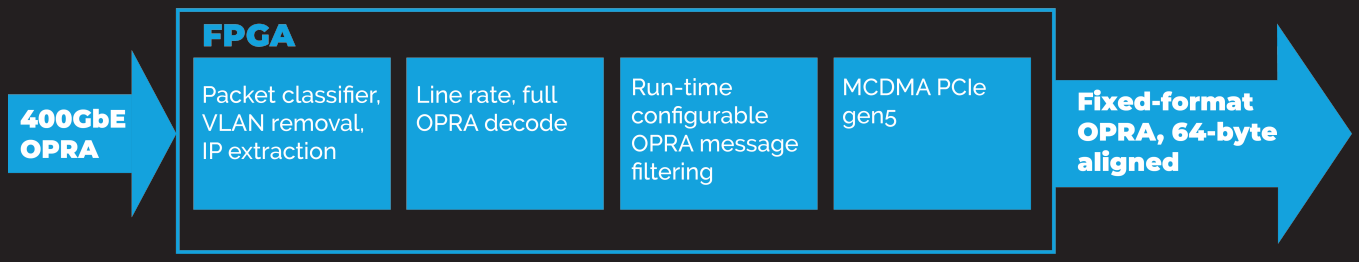
How Telesoft Can Help

FPGA IS KEY



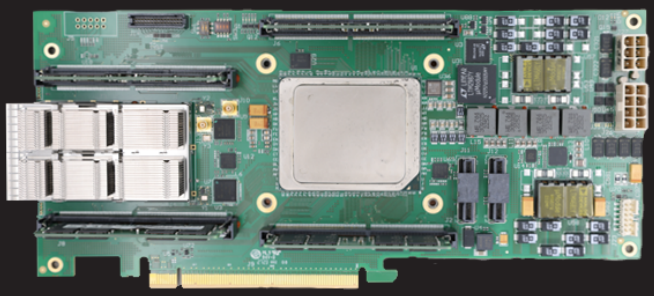
Telesoft's bespoke, accelerated FPGA capability enables sustained line-rate OPRA decode at 400Gbps, over a 400GbE interface, by utilising the following low-latency processes:

Packet Classifier
The Packet Classifier extracts each packets Internet Protocol Version and removes any VLANs. IPv4 and IPv6 are supported, as well as up to 3 VLANs.

OPRA Decode Engine
The OPRA Decode Engine extracts all short and long equity and index quote messages, equity and index last sales messages, and open interest messages from the received network traffic.

OPRA Message Filter
The OPRA Message Filter allows extracted messages to be filtered in or out, meaning only the relevant messages are passed up to the host for further processing. Messages can be filtered by participant ID, message category, message type, and session indicator.

MCDMA PCIe Gen5
Filtered messages are sent up to the host over PCIe Gen5, in a 64-byte fixed-format for efficient processing.



Our latest offering is built on the best technology:

- 2 x QSPF-DD connectors supporting 2 x 100GbE or 2 x 400GbE interfaces, providing support for A and B redundant feeds.
- Agilex I-series FPGA, coded exclusively with VHDL, ensuring the highest level of performance.
- PCIe gen5 x 16 lane interface for delivery of 400Gb of data to the host.
- Second PCIe gen5 interface for additional throughput to the host.
- Full line rate OPRA decode in FPGA with fixed format structure, 64 byte aligned for cache alignment and fastest access.
- In built FPGA block or allow list filtering for reduced host processing.
- Kernel bypass direct from DMA to user space using DPDK.
- DDR5 memory on host for low latency data manipulation.